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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
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Data processing apparatus and method

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DATA PROCESSING APPARATUS AND METHOD**Field of Invention**

The present invention relates to data processing apparatus operable to map input symbols onto carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol.

The present invention also relates to data processing apparatus operable to de-map symbols received from a predetermined number of carrier signals of an OFDM symbol into an output symbol stream.

Background of the Invention

The Digital Video Broadcasting-Terrestrial standard (DVB-T) utilises Orthogonal Frequency Division Multiplexing (OFDM) to communicate data representing video images and sound to receivers via a broadcast radio communications signal. There are known to be two modes for the DVB-T standard which are known as the 2k and the 8k mode. The 2k mode provides 2048 sub-carriers whereas the 8k mode provides 8192 sub-carriers.

In order to improve the integrity of data communicated by either the 2k mode or the 8k mode a symbol interleaver is provided in order to interleave input data symbols as these symbols are mapped onto the carrier signals of an OFDM symbol. Such a symbol interleaver comprises an interleaver memory in combination with an address generator. The address generator generates an address for each of the input symbols, each address indicating one of the carrier signals of the OFDM symbol onto which the data symbol is to be mapped. For the 2k mode and the 8k mode an arrangement has been disclosed in the DVB-T standard for generating the addresses for the mapping. The address generator is known to comprise a linear feed back shift register which is operable to generate a pseudo random bit sequence and a permutation circuit. The permutation circuit permutes the order of the content of the linear feed back shift register in order to generate an address. The address provides an indication of one of the OFDM carriers for carrying an input data symbol stored in the interleaver memory, in order to map the input symbols onto the carrier signals of the OFDM symbol.

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As well as the 2k mode and the 8k mode it has also been proposed to provide a 4k mode. The 4k mode has been used in the Japanese standard for digital broadcast television, which is the Integrated Service Digital Broadcasting (ISDB) system.

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Summary of Invention

According to an aspect of the present invention there is provided a data processing apparatus operable to map input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol. The data processing apparatus comprises an interleaver memory operable to read-in the predetermined number of data symbols for mapping onto the OFDM carrier signals, and to read-out the data symbols for the OFDM carriers to effect the mapping. The read-out is in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals. The set of addresses is determined by an address generator, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped.

The address generator comprises a linear feedback shift register including a predetermined number of register stages and is operable to generate a pseudo-random bit sequence in accordance with a generator polynomial, and a permutation circuit and a control unit. The permutation circuit is operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers. The control unit is operable in combination with an address check circuit to re-generate an address when a generated address exceeds the maximum number of carriers. The data processing apparatus is characterised in that the predetermined number of OFDM carrier signals is substantially four thousand, and the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i[10] = R_{i-1}[0] \oplus R_{i-1}[2]$. The permutation order forms an eleven bit address $R_i[n]$ for the i -th data symbol from the bit present in the n -th register stage $R_i[n]$ in accordance with the table:

$R_i[n]$ for $n =$	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for $n =$	7	10	5	8	1	2	4	9	0	3	6

Although it is known within the DVB-T standard to provide the 2k mode and the 8k mode, there are advantages in providing a 4k mode. Whilst the 8k mode

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provides an arrangement for establishing a single frequency network with sufficient guard periods to accommodate larger propagation delays between DVB transmitters, the 2k mode is known to provide an advantage in mobile applications. This is because the 2k symbol period is only one quarter of the 8k symbol period, allowing the channel estimation (based on scattered pilots embedded in each symbol) to be more frequently updated allowing the receiver to track the time variation of the channel due to doppler and other effects more accurately. The 2k mode is therefore advantageous for mobile applications. However, the 2k mode requires a multiple frequency network thereby complicating an arrangement of transmitters to provide a broadcast system. A 4k mode provides an advantage of a reasonable good reception for mobile users even at high driving speeds which thereby cause increased doppler shift, without a need for an expensive inter-carrier interference cancellation scheme. A reasonably cost effective implementation of a broadcast network can also be implemented. However, in order to provide the 4k mode a symbol interleaver must be provided for mapping the input data symbols onto the carrier signals of the OFDM symbol.

Embodiments of the present invention can provide a data processing apparatus operable as a symbol interleaver for mapping data symbols to be communicated on an OFDM symbol, having substantially four thousand carrier signals. In one embodiment the number of carrier signals is three thousand and twenty four. As such a 4k mode can be provided for example for DVB-T.

Mapping data symbols to be transmitted onto the carrier signals of an OFDM symbol, where the number of carrier signals is substantially four thousand, represents a substantial technical problem requiring simulation analysis and testing to establish an appropriate generator polynomial for the linear feedback shift register and the permutation order. This is because the mapping requires that the symbols are interleaved onto the carrier signals with the effect that successive symbols from the input data stream are separated in frequency by a greatest possible amount in order to optimise the performance of error correction coding schemes.

Error correction coding schemes such as Reed-Solomon coding and convolutional coding perform better when noise and degradation of the symbol values resulting from communication is un-correlated. Some radio channels such as those used for DVB-T may suffer from correlated fading in both the time and the frequency

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domains. As such by separating encoded symbols on to different carrier signals of the OFDM symbol by as much as possible, the performance of error correction coding schemes can be increased.

5 It has been discovered from simulation performance analysis that the generator polynomial for the linear feed back shift register in combination with the permutation circuit order indicated above, provides a good performance in the presence of typical channel noise and fading conditions. Furthermore, by providing an arrangement which can implement address generating for both the 2k mode and the 8k mode as well as the 4k mode by changing the taps of the generator polynomial for the linear feed back shift
10 register and the permutation order, a cost effective implementation of the symbol interleaver for the 4k mode is provided. Furthermore, a transmitter and a receiver can be changed between the 2k mode, 4k mode and the 8k mode by changing the generator polynomial and the permutation orders. This can be effected in software (or by the embedded transmission parameter signalling (TPS) channel in the receiver) whereby a
15 flexible implementation is provided.

Various aspects and features of the present invention are defined in the appended claims. Further aspects of the present invention include a data processing apparatus operable to de-map symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into
20 an output symbol stream, as well as a transmitter and a receiver.

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Brief Description of Drawings

Embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings, wherein like parts are provided with corresponding reference numerals, and in which:

5 Figure 1 is a schematic block diagram of a Coded OFDM transmitter which may be used, for example, with the DVB-T standard;

Figure 2 is a schematic block diagram of an inner symbol interleaver and a mapping processor which appear in Figure 1;

10 Figure 3 is a schematic block diagram of the symbol interleaver shown in Figure 2;

Figure 4 is a schematic block diagram of an interleaver memory shown in Figure 3 and the corresponding symbol de-interleaver in the receiver;

Figure 5 is a schematic block diagram of an address generator shown in Figure 3 for the 2k mode;

15 Figure 6 is a schematic block diagram of an address generator as shown in Figure 3 in the 8k mode;

Figure 7 is a schematic block diagram of an address generator shown in Figure 3 in the 4k mode;

20 Figure 8 is a schematic block diagram of a Coded OFDM receiver which may be used, for example, with the DVB-T standard; and

Figure 9 is a schematic block diagram of an inner symbol de-interleaver which appears in Figure 8.

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Description of Preferred Embodiments

The existing OFDM-based DVB-T standard is composed of a 2K and an 8K mode, which means that the bandwidth used to transmit the signal is divided into either 2048 sub-carriers (2K mode) or 8192 (8K mode). The 2K mode presents some interesting features with respect to mobility. In effect, the short symbol time of this mode allows good doppler performance in mobile environments. On the other hand, the 8K mode gives the possibility to network planners to build a sparse, hence cheap, SFNs (Single Frequency Network). The investigations carried out on the subject showed that the introduction of a 4K mode would be a good trade-off between these two modes. It would give reasonably good reception for mobile users even at high driving speeds, without the need for a complicated and costly ICI (Inter Carrier Interference) cancellation scheme. It would also help to keep the cost of the network to a reasonable level. This document describes a new symbol interleaver for this 4K mode.

Figure 1 provides an example block diagram of a Coded OFDM transmitter which may be used for example to transmit video images and audio signals in accordance with the DVB-T standard. In Figure 1 a program source generates data to be transmitted by the COFDM transmitter. A video coder 2, and audio coder 4 and a data coder 6 generate video, audio and other data to be transmitted which are fed to a program multiplexer 8. An output of the program multiplexer 8 is fed to a transport multiplexer 10 which forms a multiplexed transport stream with other information required to communicate the video, audio and other data. The transport multiplexer 10 provides a transport stream on a connecting channel 12 to a splitter 14. The splitter divides the transport stream into different branches A and B which provide different forward error correction encoding and interleaving. For simplicity, only branch A will be described.

As shown in Figure 1 a COFDM transmitter 20 receives the transport data stream at a multiplexer adaptation and energy dispersal block 22. The multiplexer adaptation and energy dispersal block 22 randomises the transport stream data and feeds the appropriate data to an outer encoder 24 which performs a first outer coding of the transport data. An outer interleaver 26 is provided to interleave the encoded

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data symbols which for the example of DVB-T is the Reed-Solomon (RS) code so that the outer interleaver interleaves RS symbols. An inner encoder 28 is arranged to convolutionally encode the data from the outer interleaver using a convolutional encoder the encoded data being fed to an inner interleaver 30. The inner interleaver 30 may also receive coded data from the second encoding arm B.

An output of the inner interleaver is a set of data symbols which are then mapped onto constellation points of a modulation scheme. For the example of the DVB-T shown, the modulation scheme is QPSK (DVB-T can have 4 bits/carrier 16QAM or 6 bits/carrier 64QAM as well as QPSK). Each data symbol from the inner interleaver 30 is then mapped onto one of the COFDM carrier signals by a mapping processor 32. The COFDM symbol is then generated by a frame adaptation processor 34 which introduces pilot and synchronising signals fed from a signal former 36. An OFDM generator 38 then forms the OFDM symbol in the time domain which is fed to a guard insertion processor 40 for generating a guard interval between symbols, and then to a digital to analogue convertor 42 and finally to an RF amplifier within an RF front 44 for eventual broadcast by the COFDM transmitter from an antenna 46.

To create a new 4K mode, several elements are to be defined, but the main one is the 4K symbol interleaver, which is part of the inner interleaver shown in Figure 1.

The inner interleaver itself is composed of a bit interleaver and a symbol interleaver as shown in Figure 2.

As explained above, the present invention provides a facility for providing a quasi-optimal mapping of the input data symbols onto the OFDM carrier signals. According to the example technique the inner interleaver is provided to effect the optimal mapping of input data symbols onto COFDM carrier signals. The inner interleaver 30 and the mapping processor 32 are shown in Figure 2 in more detail. In Figure 2 the inner interleaver 30 comprises a de-multiplexing processor 60 which receives convolutionally encoded bits from an input channel 62. The de-multiplexer then divides the bits into two streams of input bits which are fed via connecting channels 64 and 66 to bit interleavers 68 and 70. The bit interleavers interleave the bits which are then formed on two connecting channels 72.1, 72.2 for connecting the bits from each of the bit interleavers 68 and 70 to a symbol interleaver 76. The symbol interleaver forms the input symbols from the connecting channels 72.1, 72.2 into

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symbols for mapping onto the COFDM carrier signals. For the example technique shown in Figure 2 the interleaved symbols from the symbol interleaver 76 are mapped onto constellation points of a QPSK carrier signal for each of the signals in the COFDM symbol.

- 5 The existing DVB-T specification already defines a symbol interleaver for the 2K and 8K modes. The purpose of the symbol interleaver is to map v bit words (v depending on the modulation scheme chosen) onto the 1 512 (2K mode) or 6 048 (8K mode) active carriers per OFDM symbol. The symbol interleaver acts on blocks of 1 512 (2K mode) or 6 048 (8K mode) data symbols. Example embodiments of the
- 10 present invention utilise the symbol interleaver 76 to provide an optimised mapping of the input data symbols fed from the connecting channels 72.1, 72.2 onto the COFDM carrier signals. An example of the symbol interleaver 76 for effecting mapping of the input data symbols onto the COFDM carrier signals is shown in Figure 3.

Interleaver RAM

- 15 In Figure 3 the input data symbols from the connecting channel 72 are fed to an interleaver memory 100. The interleaver memory 100 maps the input data symbols onto the COFDM carrier signals in accordance with mapping addresses provided by address generator 102. An example implementation of the interleaver memory 100 is shown in Figure 4.

- 20 The interleaver memory shown in Figure 4 comprises an upper part 100 illustrating the operation of an interleaver in the transmitter and a lower part 340 which illustrates the operation of a de-interleaver in the receiver. The interleaver 100 and the de-interleaver 340 are shown together in Figure 4 in order to facilitate understanding of their operation. As shown in Figure 4 a representation of the communication
- 25 between the interleaver 100 and the de-interleaver 340 via other devices and via a transmission channel has been simplified and represented as a section 140 between the interleaver 100 and the de-interleaver 340. The operation of the interleaver 100 is described in the following paragraphs:

- 30 Although Figure 4 provides an illustration of only four input data symbols onto an example of four carrier signals of a COFDM symbol, it will be appreciated that the

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technique illustrated in Figure 4 can be extended to a larger number of carriers such as 1512 for the 2k mode, 3024 for the 4k mode and 6048 for the 8k mode.

The input and output addressing of the interleaver memory 100 shown in Figure 4 is shown for odd and even symbols. For an even COFDM symbol the data symbols are read from the input channel 72 in accordance with a sequence of addresses 120 generated for each COFDM symbol by the address generator 102 into an interleaver RAM 124.1. The data symbols read into the interleaver RAM 124 are then read out in sequential order 126. The addresses are applied to the read in order for the even symbol so that as illustrated an interleaving is effected by the read in addresses. Therefore, for each interleaved symbol $y(h(q)) = y'(q)$.

For odd symbols the same interleaver RAM 124.2 is used. However, as shown in Figure 4 for the odd symbol the read in order 132 is in the same sequential address sequence used to read out the previous even symbol 126. This feature allows the transmitter and receiver implementations to only use 1 RAM provided the read-out operation for a given address is performed before the read-in operation. The data symbols read into the interleaver RAM 124 are then read out in a sequence 134 generated in accordance with the addresses generated by the address generator for each COFDM symbol by address generator 102

In summary, as represented in Figure 4, once the set of addresses $H(q)$ has been calculated for all active carriers, the input vector $Y' = (y_0', y_1', y_2', \dots, y_{N_{\max}-1}')$ is processed to produce the interleaved vector $Y = (y_0, y_1, y_2, \dots, y_{N_{\max}-1})$ defined by:

$$y_{H(q)} = y'_q \text{ for even symbols for } q = 0, \dots, N_{\max}-1$$

$$y_q = y'_{H(q)} \text{ for odd symbols for } q = 0, \dots, N_{\max}-1$$

In other words, for even OFDM symbols the input words are written in a permuted way into a memory and read back in a straight way, whereas for odd symbols, they are written straight and read back permuted. In the above case, the permutation $H(q)$ is defined by the following table:

q	1	2	3	4
H(q)	1	3	0	2

Table 1: permutation for simple case where $N_{\max} = 4$

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As shown in Figure 4, the de-interleaver 340 operates to reverse the interleaving applied by the interleaver 100, by applying the same set of addresses as generated by an equivalent address generator, but applying the read-in and read-out addresses in reverse. As such, for even symbols, the read in addresses 342 are in sequential order, whereas the read out address 344 are provided by the address generator. Correspondingly, for the odd symbols, the read in order 346 is determined from the set of addresses generated by the address generator, whereas read out 348 is in sequential order.

Address Generation

10 A schematic block diagram of the algorithm used to generate the permutation function $H(q)$ is represented in Figure 5 for the 2K mode and in Figure 6 for the 8K mode.

An implementation of the address generator 102.1 for the 2k mode is shown in Figure 5. In Figure 5 a linear feed back shift register is formed by ten register stages 200.1 and a xor-gate 202.1 which is connected to the stages of the shift register 200.1 in accordance with a generator polynomial. Therefore, in accordance with the content of the shift register 200.1 a next bit of the shift register is provided from the output of the xor-gate 202.1 by xoring the content of shift register $R[0]$ and register stage $R[3]$. According to the generator polynomial a pseudo random bit sequence is generated from the content of the shift register 200.1. However, in order to generate an address for the 2k mode as illustrated, a permutation circuit 210.1 is provided which effectively permutes the order of the bits within the shift register 200.1 from an order $R'_i[n]$ to an order $R_i[n]$ at the output of the permutation circuit 210.1. Ten bits from the output of the permutation circuit 210.1 are then fed on a connecting channel 212.1 to which is added a most significant bit via a channel 214.1 which is provided by a toggle circuit 218.1. An eleven bit address is therefore generated on channel 212.1. However, in order to ensure the authenticity of an address, an address check circuit 216.1 analyses the generated address to determine whether it exceeds the maximum number of carrier signals. If it does then a control signal is generated and fed via a connecting channel 220.1 to a control unit 224.1. If the generated address exceeds the

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maximum number of carrier signals then this address is rejected and a new address regenerated for the particular symbol.

An address generator 102 for the 8k mode is shown in Figure 6. The parts of the address generator for the 8k mode shown in Figure 6 correspond to those shown for the 2k mode and so to avoid repetition only essential differences between Figure 6 and Figure 5 will be described. Essentially, the difference between Figure 6 and Figure 5 is that the linear feed back shift register 200.2 has twelve shift register stages in order to generate an address between 0 and 8191. Again, the shift register is formed from xoring the shift register stages selected in accordance with the generator polynomial. The address is then formed by permuting the order of the bits within the shift register 200.2 which is determined in accordance with a predetermined order. Again, the generator polynomial and the permutation order is provided for the 8k mode which differs from the 2k mode.

In summary for the 2k and 8k modes an $(N_T - 1)$ bit word R'_i is defined, with $N_T = \log_2 M_{\max}$, where $M_{\max} = 2\,048$ in the 2K mode and $M_{\max} = 8\,192$ in the 8K mode, using a LFSR (Linear Feedback Shift Register).

The polynomials used to generate this sequence are as follows:

$$2K \text{ mode: } R'_i[9] = R'_{i-1}[0] \oplus R'_{i-1}[3]$$

$$8K \text{ mode: } R'_i[11] = R'_{i-1}[0] \oplus R'_{i-1}[1] \oplus R'_{i-1}[4] \oplus R'_{i-1}[6]$$

where i varies from 0 to $M_{\max} - 1$

Once one R'_i word has been generated, it goes through a permutation to produce another $(N_T - 1)$ bit word called R_i . R_i is derived from R'_i by the bit permutations given in tables 1 and 2.

R'_i bit positions	9	8	7	6	5	4	3	2	1	0
R_i bit positions	0	7	5	1	8	2	6	9	3	4

Table 2: Bit permutation for the 2K mode

R'_i bit positions	11	10	9	8	7	6	5	4	3	2	1	0
R_i bit positions	5	11	3	0	10	8	6	9	2	4	1	7

Table 3: Bit permutation for the 8K mode

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As an example, this means that for mode 2K, the bit number 9 of R_i is sent in bit position number 0 of R_i .

The address $H(q)$ is then derived from R_i through the following equation:

$$H(q) = (i \bmod 2) \cdot 2^{N_r-1} + \sum_{j=0}^{N_r-2} R_i(j) \cdot 2^j$$

5 The $(i \bmod 2) \cdot 2^{N_r-1}$ part of the above equation is represented in Figure 5 and in Figure 6 by the toggle block T 218.

An address check is then performed on $H(q)$ to verify that the generated address is within the range of acceptable addresses: if $(H(q) < N_{\max})$, where $N_{\max} = 1512$ in the 2K mode and 6048 in the 8K mode, then the address is valid. If the
10 address is not valid, the control unit is informed and it will try to generate a new $H(q)$ by incrementing the index i .

The role of the toggle block is to make sure that we do not generate an address exceeding N_{\max} twice in a row. In effect, if an exceeding value was generated, this means that the MSB (i.e. the toggle bit) of the address $H(q)$ was one. So the next value
15 generated will have a MSB set to zero, insuring to produce a valid address.

The following equations sum up the overall behaviour and help to understand the loop structure of this algorithm:

20 $q = 0;$
for ($i = 0; i < M_{\max}; i = i + 1$)
 $\{ H(q) = (i \bmod 2) \cdot 2^{N_r-1} + \sum_{j=0}^{N_r-2} R_i(j) \cdot 2^j;$
if ($H(q) < N_{\max}$) $q = q + 1;$ }

Symbol Interleaver for 4k Mode

25 According to the present technique an address generator 102.3 for the 4k mode is shown in Figure 7. Again, the address generator of Figure 7 corresponds to the address generator shown in Figures 5 and 6 and so the only differences between these Figures will be discussed and explained. As shown in Figure 7 the linear feed back shift register 200.3 has eleven shift register stages. Again, an xor-gate 202.3 is

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provided to generate the pseudo random bit sequence. The permutation of the contents of the shift register in order to form the address of an input data symbol for mapping onto one of the COFDM carrier signals is provided by the permutation circuit 210.3.

The symbol interleaver acts on blocks of $N_{\max} = 3024$ data symbols. ($M_{\max} =$
5 4096).

The polynomial used to generate the R'_i sequence is:

$$R'_i[10] = R'_{i-1}[0] \oplus R'_{i-1}[2]$$

A vector R_i is derived from the vector R'_i by the bit permutation given in Table
4:

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R'_i bit positions	10	9	8	7	6	5	4	3	2	1	0
R_i bit positions	7	10	5	8	1	2	4	9	0	3	6

Table 4: Bit permutation for the 4K mode

The input of the interleaver is defined as the vector $Y' = (y_0', y_1',$
 $y_2', \dots, y_{N_{\max}-1}')$.

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The interleaved vector $Y = (y_0, y_1, y_2, \dots, y_{N_{\max}-1})$ is defined by:

$$y_{H(q)} = y'_q \text{ for even symbols for } q = 0, \dots, N_{\max}-1$$

$$y_q = y'_{H(q)} \text{ for odd symbols for } q = 0, \dots, N_{\max}-1$$

Receiver

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Figure 8 provides an example illustration of a receiver which may be used with the present technique. As shown in Figure 8, a COFDM signal is received by an antenna 300 and detected by a tuner 302 and converted into a digital form by an analogue-to-digital converter 304. A guard interval removal processor 306 removes the guard interval from a received COFDM symbol, before the data is recovered from the COFDM symbol using a Fast Fourier Transform (FFT) processor 308 in combination with a pilot extraction processor 310 in co-operation with a pilot and Transmission Parameter Signalling (TPS) channel processing unit 311, in accordance with known techniques. The demodulated data is recovered from a de-mapper 312 and

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fed to an inner symbol de-interleaver 314, which operates to effect the reverse mapping of the received data symbol to re-generate an output data stream with the data de-interleaved.

The symbol de-interleaver 314 is formed from a data processing apparatus as shown in Figure 9 with an interleaver memory 340 and an address generator 342. The interleaver memory is as shown in Figure 4 and operates as already explained above to effect de-interleaving by utilising sets of addresses generated by the address generator 342. The address generator 342 is formed as shown in Figure 7 and is arranged to generate corresponding addresses to map the data symbols recovered from each COFDM sub-carrier signals into an output data stream.

The remaining parts of the COFDM receiver shown in Figure 8 are provided to effect error correction decoding and de-interleaving to correct errors and recover an estimate of the source data. In particular, an inner-code de-interleaver 316 and an inner-decoder 318 operate to effect decoding of the inner convolutional code introduced by the inner interleaver 30 and the inner coder 28 of the receiver shown in Figure 1. An outer de-interleaver 320 and an outer decoder 322 operate to effect decoding of the Reed-Solomon code to recover an estimate of the data from the source 1, after being descrambled by a descrambler 324.

One advantage provided by the present technique for both the receiver and the transmitter is that a symbol interleaver and a symbol de-interleaver operating in the receivers and transmitters can be switched between the 2k, 8k and the 4k mode by changing the generator polynomials and the permutation order. A flexible implementation is thereby provided because a symbol interleaver and de-interleaver can be formed as shown in Figures 4 and 9, with an address generator as illustrated in either of Figures 5, 6 or 7. The address generator can therefore be adapted to the different modes by changing to the generator polynomials and the permutation orders indicated for each of the 2k, 4k, and 8k modes. For example this can be effected using a software change. Alternatively, in other embodiments, an embedded TPS signal indicating the mode of the DVB-T transmission can be detected in the receiver in the TPS channel processing unit 311 and used to configure automatically the symbol de-interleaver in accordance with the detected mode.

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Various modifications may be made to the embodiments described above without departing from the scope of the present invention. In particular, the example representation of the generator polynomial and the permutation order which have been used to represent aspects of the invention are not intended to be limiting and extend to
5 equivalent forms of the generator polynomial and the permutation order.

As will be appreciated the transmitter and receiver shown in Figures 1 and 8 respectively are provided as illustrations only and are not intended to be limiting. For example, it will be appreciated that the position of the symbol interleaver and the de-interleaver with respect, for example to the bit interleaver and the mapper and de-mapper. As will be appreciated the effect of the interleaver and de-interleaver is un-
10 changed by its relative position, although the interleaver may be interleaving I/Q symbols instead of v-bit vectors. A corresponding change may be made in the receiver. Accordingly the interleaver and de-interleaver may be operating on different data types, and may be positioned differently to the position described in the example
15 embodiments.

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[1] EN 300 744, "Framing structure, channel coding and modulation for digital terrestrial television", ETSI

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1. A data processing apparatus operable to map input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the data processing apparatus comprising

an interleaver memory operable to read-in the predetermined number of data symbols for mapping onto the OFDM carrier signals, and to read-out the data symbols for the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to regenerate an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i[10] = R_{i-1}[0] \oplus R_{i-1}[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the bit present in the n-th register stage $R_i[n]$ in accordance with the table:

$R_i[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

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2. A data processing apparatus as claimed in Claim 1, wherein the predetermined number of carrier signals is three thousand and twenty four.

3. A data processing apparatus as claimed in Claim 1 or 2, wherein the interleaver memory is operable to effect the mapping of the input data symbols onto the carrier signals for even OFDM symbols by reading in the data symbols according to the set of addresses generated by the address generator and reading out in a sequential order, and for odd OFDM symbols by reading in the symbols into the memory in a sequential order and reading out the data symbols from the memory in accordance with the set of addresses generated by the address generator.

4. A transmitter for transmitting data using Orthogonal Frequency Division Multiplexing (OFDM), the transmitter including a data processing apparatus according to any preceding Claim.

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5. A transmitter as claimed in Claim 4, wherein the transmitter is operable to transmit data in accordance with the Digital Video Broadcasting-Terrestrial standard.

6. A data processing apparatus operable to de-map symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the data processing apparatus comprising

a de-interleaver memory operable to read-in the predetermined number of data symbols from the OFDM carrier signals, and to read-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

an address generator operable to generate the set of addresses, an address being generated for each of the received data symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the address generator comprising

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a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

5 a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

a control unit operable in combination with an address check circuit to regenerate an address when a generated address exceeds the predetermined number of carriers, characterised in that

10 the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R'_i[10] = R'_{i-1}[0] \oplus R'_{i-1}[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i-th data symbol from the

15 bit present in the n-th register stage $R'_i[n]$ in accordance with the table:

$R'_i[n]$ for n =	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for n =	7	10	5	8	1	2	4	9	0	3	6

7. A data processing apparatus as claimed in Claim 6, wherein the predetermined number of carrier signals is three thousand and twenty four.

20 8. A data processing apparatus as claimed in Claim 6 or 7, wherein the de-interleaver memory is arranged to effect the de-mapping of the received data symbols from the carrier signals onto the output data stream for even OFDM symbols by reading in the data symbols according to a sequential order and reading out the data symbols from memory according to the set of addresses generated by the address
25 generator, and for odd OFDM symbols by reading in the symbols into the memory in accordance with the set of addresses generated by the address generator and reading out the data symbols from the memory in accordance with a sequential order.

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9. A receiver for receiving data from Orthogonal Frequency Division Multiplexing (OFDM) modulated signal, the receiver including a data processing apparatus according to any of Claims 6, 7 or 8.

5 10. A receiver as claimed in Claim 9, wherein the receiver is operable to receive data which has been modulated in accordance with the Digital Video Broadcasting-Terrestrial standard.

10 11. A method of mapping input symbols to be communicated onto a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol, the method comprising

reading-in the predetermined number of data symbols for mapping onto the OFDM carrier signals,

15 reading-out the data symbols for the OFDM carriers to effect the mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are interleaved on the carrier signals,

generating the set of addresses, an address being generated for each of the input symbols to indicate one of the carrier signals onto which the data symbol is to be mapped, the generating the set of addresses comprising

20 using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

25 using a permutation circuit operable to receive the content of the shift register stages to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the of OFDM carriers, and

re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

30 the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R'_i[10] = R'_{i-1}[0] \oplus R'_{i-1}[2]$, and the

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permutation order forms an eleven bit address $R_i[n]$ for the i -th data symbol from the bit present in the n -th register stage $R'_i[n]$ in accordance with the table:

$R'_i[n]$ for $n =$	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for $n =$	7	10	5	8	1	2	4	9	0	3	6

12. A method of de-mapping symbols received from a predetermined number of carrier signals of an Orthogonal Frequency Division Multiplexed (OFDM) symbol into an output symbol stream, the method comprising

reading-in the predetermined number of data symbols from the OFDM carrier signals,

reading-out the data symbols into the output symbol stream to effect the de-mapping, the read-out being in a different order than the read-in, the order being determined from a set of addresses, with the effect that the data symbols are de-interleaved from the OFDM carrier signals,

generating the set of addresses, an address being generated for each of the received symbols to indicate the OFDM carrier signal from which the received data symbol is to be de-mapped into the output symbol stream, the generating the set of addresses comprising

using a linear feedback shift register including a predetermined number of register stages to generate a pseudo-random bit sequence in accordance with a generator polynomial,

using a permutation circuit to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and

re-generating an address when a generated address exceeds the predetermined number of carriers, characterised in that

the predetermined number of OFDM carrier signals is substantially four thousand,

the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R'_i[10] = R'_{i-1}[0] \oplus R'_{i-1}[2]$, and the

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permutation order forms an eleven bit address $R_i[n]$ for the i -th data symbol from the bit present in the n -th register stage $R_i[n]$ in accordance with the table:

$R_i[n]$ for $n =$	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for $n =$	7	10	5	8	1	2	4	9	0	3	6

- 5 13. An address generator for use with transmission or reception of data symbols interleaved onto substantially four thousand carriers of an Orthogonal Frequency Division Multiplexed symbol, the address generator being operable to generate a set of addresses, each address being generated for each of the data symbols to indicate one of the carrier signals onto which the data symbol is to be mapped or de-
- 10 mapped, the address generator comprising

a linear feedback shift register including a predetermined number of register stages and being operable to generate a pseudo-random bit sequence in accordance with a generator polynomial,

- a permutation circuit operable to receive the content of the shift register stages and to permute the bits present in the register stages in accordance with a permutation order to form an address of one of the OFDM carriers, and
- 15

a control unit operable in combination with an address check circuit to regenerate an address when a generated address exceeds the predetermined number of carriers, characterised in that

- 20 the linear feedback shift register has eleven register stages with a generator polynomial for the linear feedback shift register of $R_i[10] = R_{i-1}[0] \oplus R_{i-1}[2]$, and the permutation order forms an eleven bit address $R_i[n]$ for the i -th data symbol from the bit present in the n -th register stage $R_i[n]$ in accordance with the table:

$R_i[n]$ for $n =$	10	9	8	7	6	5	4	3	2	1	0
$R_i[n]$ for $n =$	7	10	5	8	1	2	4	9	0	3	6

- 25 14. A data processing apparatus operable to map data symbols according to Figure 4, a data processing apparatus according to Figure 9 operable to de-map symbols received, an address generator according to Figure 7, a transmitter according

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to Figure 1, or a receiver according to Figure 8 substantially as herein before described with reference to these accompanying drawings.

15. A method of mapping input symbols to be communicated onto a
5 predetermined number of carrier signals of an Orthogonal Frequency Division
Multiplexed (OFDM) symbol, and a method of de-mapping symbols received from a
predetermined number of carrier signals of an Orthogonal Frequency Division
Multiplexed (OFDM) symbol into an output symbol stream, substantially as herein
before described with reference to Figures 1 to 4 and 7 to 9.

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- 3. 04. 2003
(54)**ABSTRACT****DATA PROCESSING APPARATUS AND METHOD**

A data processing apparatus maps input symbols to be communicated onto a
5 predetermined number of carrier signals of an Orthogonal Frequency Division
Multiplexed (OFDM) symbol. The data processor includes an interleaver memory
which reads-in the predetermined number of data symbols for mapping onto the
OFDM carrier signals. The interleaver memory reads-out the data symbols on to the
OFDM carriers to effect the mapping, the read-out being in a different order than the
10 read-in, the order being determined from a set of addresses, with the effect that the
data symbols are interleaved on the carrier signals. The set of addresses are generated
from an address generator which comprises a linear feedback shift register and a
permutation circuit. In order to provide a 4k mode for an OFDM modulated system
such as the Digital Video Broadcasting-Terrestrial (DVB-T) standard, a generator
15 polynomial for the linear feedback shift register of $R'_i[10] = R'_{i-1}[0] \oplus R'_{i-1}[2]$ is provided
with a permutation order which has been established by simulation analysis to
optimise communication performance via typical radio channels.

[Fig. 7]

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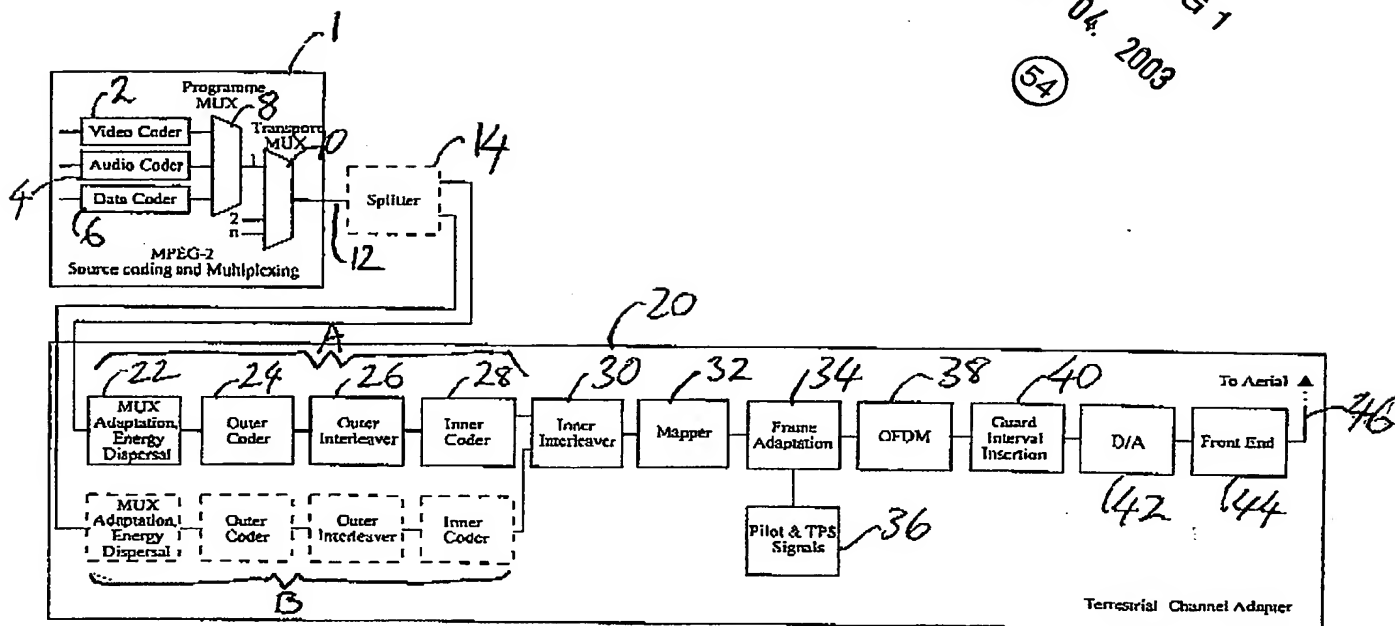
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- 3. 04. 2003
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Fig. 1

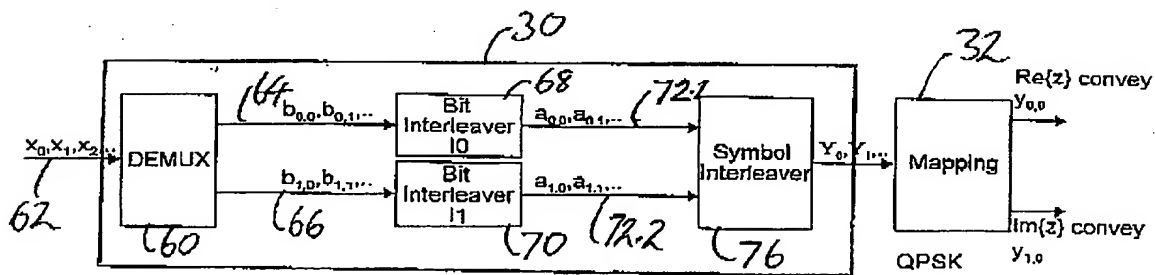


Fig. 2

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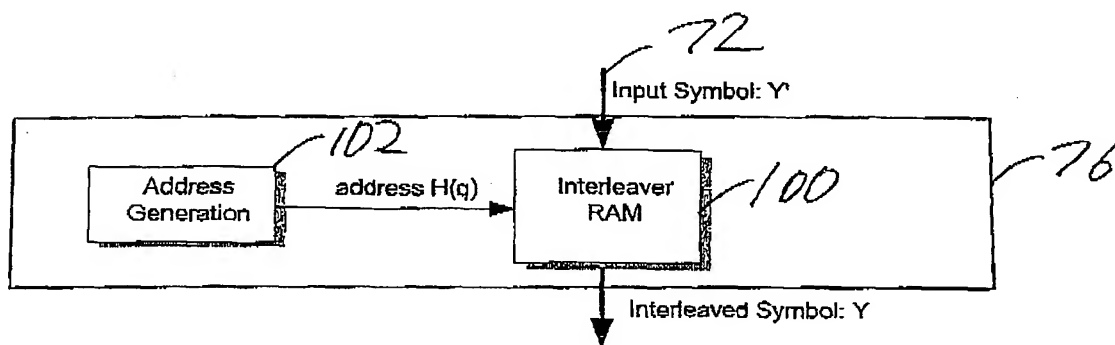


Fig. 3

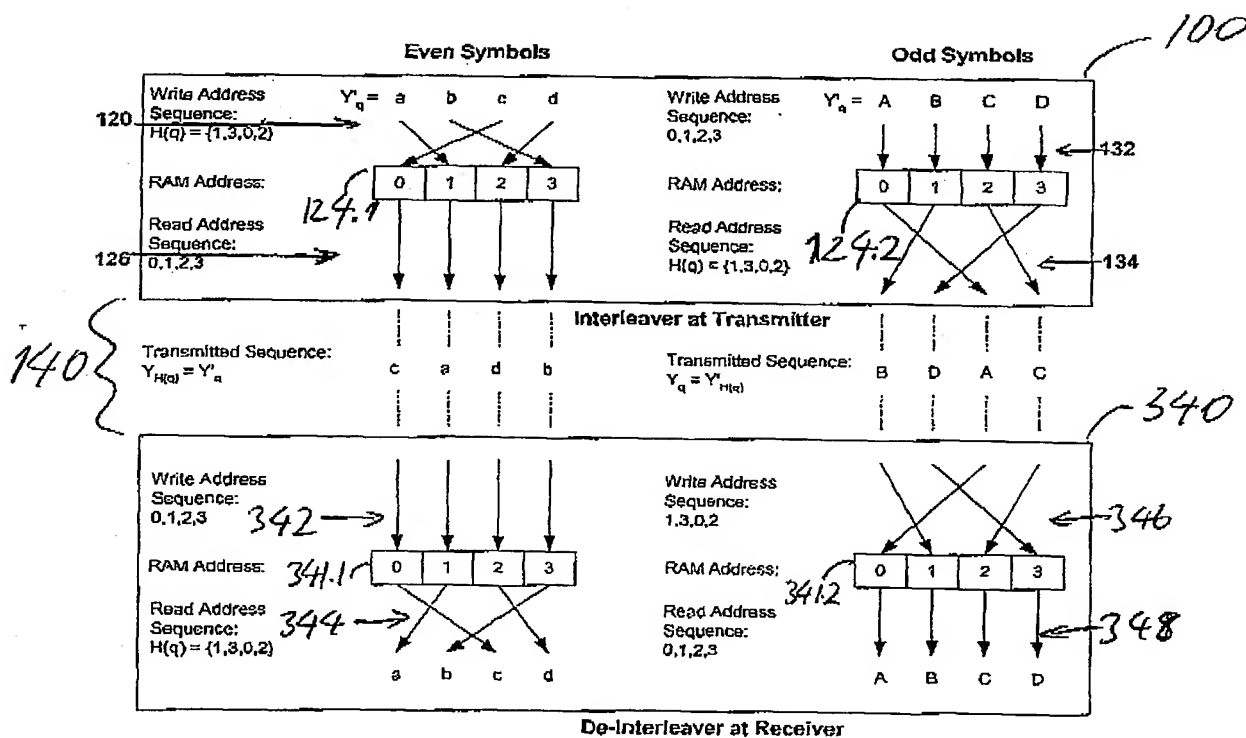
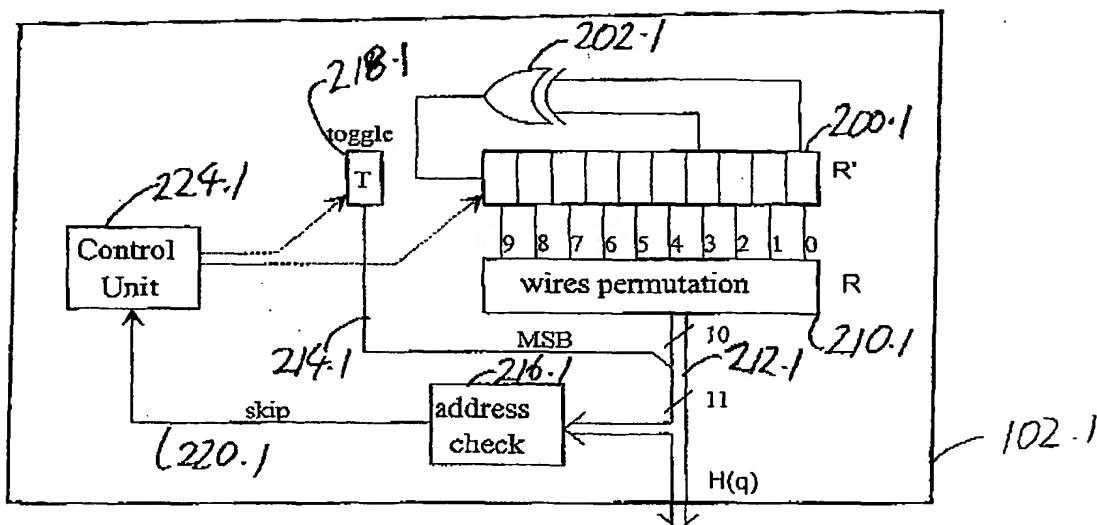


Fig 4

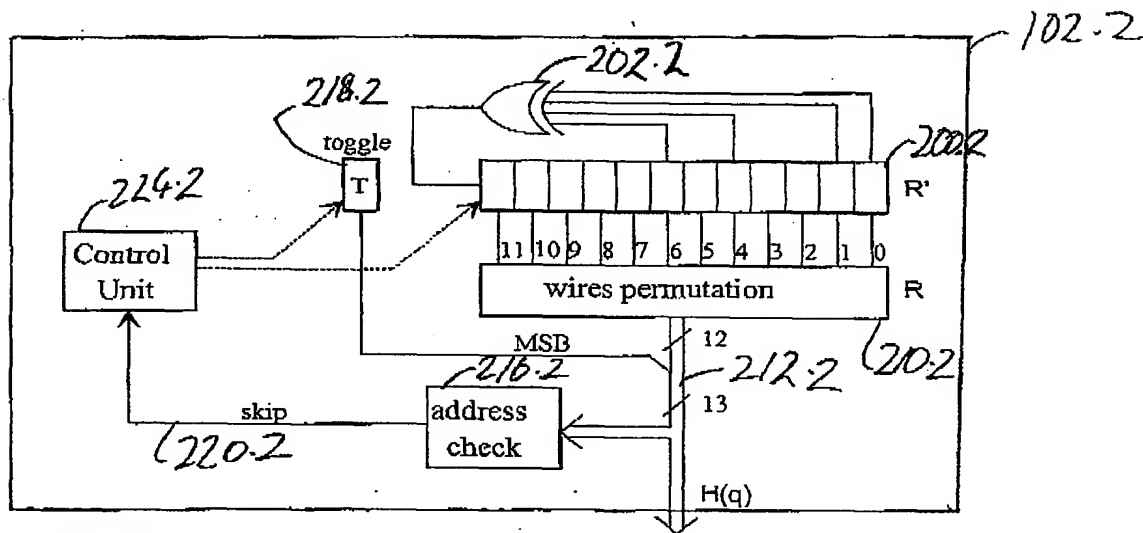
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2K Mode

Fig 5



8K Mode

Fig 6

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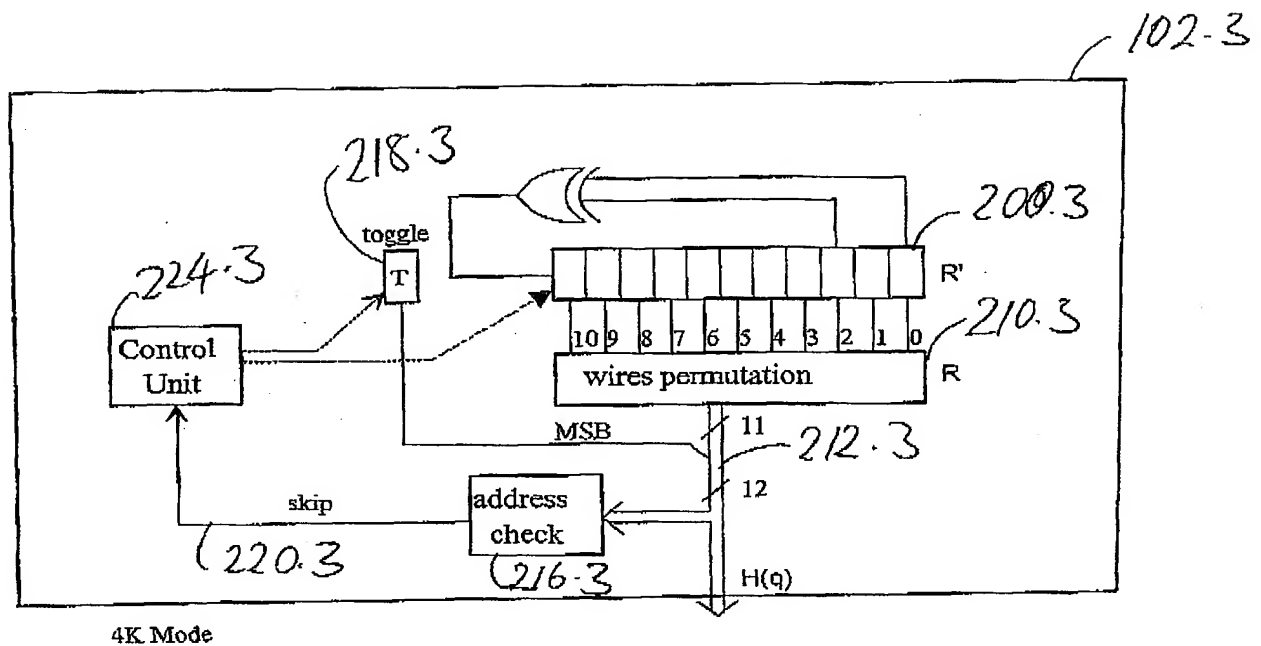


Fig 7

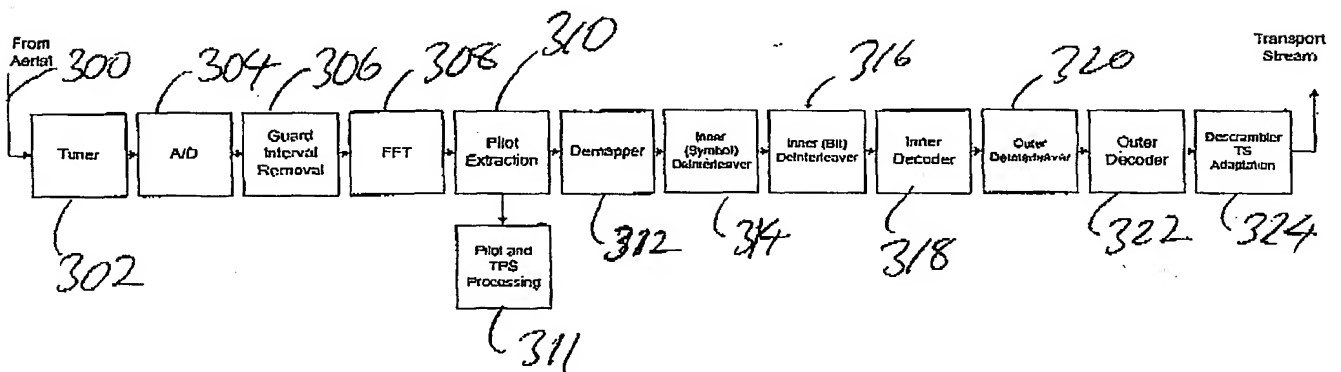


Fig 8

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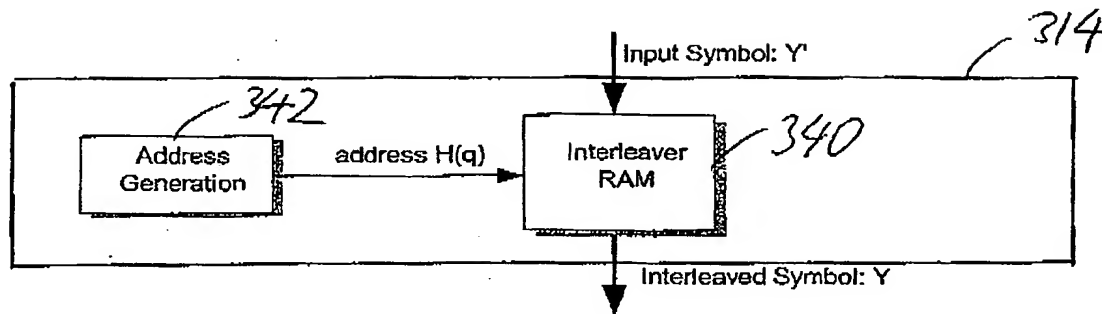


Fig. 9

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